The diagram shows good agreement with Hopfer [11] for $a/b = 0.5$ and $a/b = 0.9$ which were the only available data for thin ridges.

The analysis assumes infinitely thin ridges. A practical ridge, especially in the (b)-type guide of Fig. 1, has a certain thickness. The effect of that makes $Z_{0\infty}$ smaller and λ_c longer, i.e., the same as for a narrower slot.

The single-ridged waveguide has the same cutoff wavelength but half the characteristic impedance as those of the corresponding double-ridged waveguide.

The feeding of the shielded slot line can be accomplished in several ways. Most interesting is the case when the feeding line is of stripline type. The single-ridged guide is fed by a strip connected straight on the ridge. To feed the double-ridged guide at the ridges, two strips carrying the opposite phase are needed. It can also be fed by a single strip passing perpendicularly under the slot in the same way as slot antennas are fed by striplines [15].

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An Approximate Comparison Between n^+-p-p^+ and p^+-n-n^+ Silicon TRAPATT Diodes

G. I. HADDAD, C. M. LEE, and W. E. SCHROEDER

***Abstract*—The difference in the ionization rates of holes and electrons in Si results in different properties of n^+-p-p^+ and p^+-n-n^+ TRAPATT diodes. An approximate analysis is presented which shows these differences and indicates superior performance in the n^+-p-p^+ structure.**

The avalanche region width in various avalanche-diode structures was considered by Schroeder and Haddad and presented elsewhere [1]. Based on these results, Haddad suggested in 1971 that n^+-p-p^+ Si diodes should be better in the TRAPATT mode than the more commonly employed p^+-n-n^+ ones, especially at lower current densities which are appropriate for CW operation. The reasons for this suggestion were presented elsewhere [2]. Recently, Bierig *et al.* [3] have conducted an experimental comparison between the two types of structures in the TRAPATT mode and have shown that the n^+-p-p^+ diode has superior performance concerning efficiency and power output and were able to obtain CW operation in these structures much more easily than the conventional p^+-n-n^+ ones. The reasons for this, as suggested previously [2] are, as follows.

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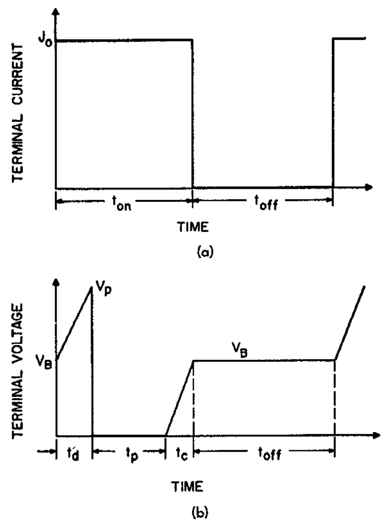

Fig. 1. Device current and voltage waveforms.

1) Since the avalanche region width in the n^+-p-p^+ structure is much narrower than that in the p-$^+$n-n^+ one [1], especially for high punch-through factor diodes which are appropriate for TRAPATT operation, the IMPATT performance for these diodes should be superior, and thus, it should be easier to generate the overvoltage required for initiation of the trapped plasma mode at current densities which are appropriate for CW operation.

2) As will be shown in the approximate analysis presented here, the delay time and thus the overvoltage are lower for the n-$^+$p-p^+ structure. This leads to better efficiency, especially at current densities which are appropriate for CW operation.

The analysis presented here should be considered very approximate, and a more exact analysis is presently underway to determine the validity of the various approximations. It is based on three articles which have been published elsewhere. These include the work by Schroeder and Haddad [1] concerning the avalanche region width, the work by Evans [4] and in particular his approximate expression for the delay time and overvoltage, and the work by DeLoach and Scharfetter [5] concerning the recovery time after the initiation of a dense plasma.

In this analysis, the terminal current of the diode is assumed to have the waveform shown in Fig. 1(a), and the corresponding terminal voltage is approximated by the waveform shown in Fig. 1(b), where

- t_d the delay time;
- t_p the recovery time;
- t_c the diode charging time;
- t_{on} the on time;
- t_{off} the off time.

The diode terminal voltage at the beginning of the cycle is chosen to be the diode dc breakdown voltage V_B. The on time t_{on} is chosen to be $t_{on} = t_d + t_p + t_c$, and the off time t_{off} is chosen to be equal to t_{on}. The waveform shown in Fig. 1 is rather idealized but does give reasonable results at the fundamental frequency and has been employed by others [4]–[6].

To carry out the analysis, the breakdown voltage V_B and the avalanche region width $\bar{w}$ for a particular diode structure are obtained in a manner described elsewhere [1]. Then the delay time t_d and the peak voltage V_p are calculated by solving Evans' [4] equations

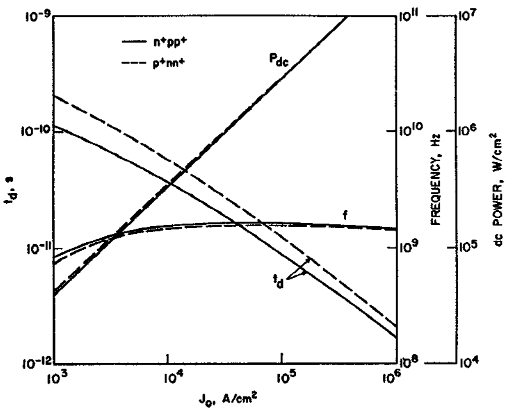

Fig. 2. Delay time, frequency, and dc power dissipated versus J_0. ($w=4$ μm and punch-through factor $F=2$. n-type: doping $=2.8\times10^{15}$, $\bar{w}/w=0.62$, $V_B=104.8$. p-type: doping $=3\times10^{15}$, $\bar{w}/w=0.18$, $V_B=107.8$.)

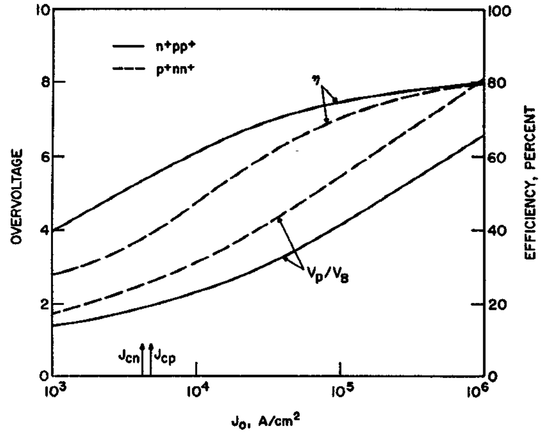

Fig. 3. Efficiency and overvoltage versus J_0. ($w=4$ μm and $F=2$. n-type: doping $=2.8\times10^{15}$, $\bar{w}/w=0.62$, $V_B=104.8$. p-type: doping $=3\times10^{15}$, $\bar{w}/w=0.18$, $V_B=107.8$.)

which are given by

$$t_d = \frac{\epsilon}{\lambda J_0}\ln\left[1+\frac{\lambda J_0}{\epsilon}\left(t_d+\frac{\bar{w}}{2v_s}\ln\frac{J_0}{J_s}\right)\right] \tag{1}$$

and

$$V_p = V_B + \frac{wJ_0}{\epsilon}t_d \tag{2}$$

where

- λ the constant in $\alpha=A_0\exp(\lambda E)$; for silicon, the value of λ has been chosen [4] to be 0.333×10^{-5} cm/V;
- J_0 total current density during the first half cycle;
- J_s the reverse saturation current density (a value of 1 A/cm² is taken for J_s in this study);
- $\bar{w}$ the avalanche region width defined as the width where the majority particle current reaches 85 percent of the total current when the diode is reverse biased into breakdown;
- w the diode width;
- v_s the saturated velocities of carriers (v_s is assumed to be 1×10^7 cm/s in this study).

The recovery time t_p is obtained by using DeLoach and Scharfetter's [5] equation

$$t_p = \frac{w}{2v_p}+\frac{w}{2v_s} \tag{3}$$

where

$$v_p = v_s\frac{J_0}{J_p} \tag{4}$$

and J_p, the peak value of the particle current, is obtained by solving

$$\frac{J_p}{J_s} = \exp\left(\frac{J_p}{J_0}\right). \tag{5}$$

t_c is the time needed to charge the diode by the current J_0 from zero to V_B V and is given by

$$t_c = \frac{\epsilon}{w}\frac{V_B}{J_0}. \tag{6}$$

The on time and off time are

$$t_{on} = t_d + t_p + t_c = t_{off}. \tag{7}$$

Now that the waveforms have been determined, a Fourier analysis can be carried out to determine the power output and efficiency. Calculations have been carried out on various structures and typical results are given in Figs. 2 and 3. It is shown in Fig. 2 that for a given current density, the delay time t_d is smaller for the n-+p-p+ structure, and thus the overvoltage is smaller. This results in an improved efficiency as can be seen in Fig. 3. It is also shown in Fig. 3 that the efficiency achievable in the n-+p-p+ structure is greater, particularly at lower current densities where CW operation is possible. It has been pointed out [5], [6] that a minimum current density is usually required to initiate an avalanche shock front and a trapped plasma which is given by $J_c=qv_sN_d$. These minimum current densities for the n and p diodes, J_{cn} and J_{cp}, respectively, are indicated in Fig. 3. Thus, it may be argued that these results are only applicable for values of $J_0>J_c$. However, it was pointed out by Evans [4], based on computer experiments, that the main features of the trapped plasma mode are retained even for values of $J_0<J_c$ (by a factor of two or more).

Based on these approximate results, it can be concluded that n-+p-p+ Si diodes are superior to p-+n-n+ ones in the TRAPATT mode. The approximate results obtained here are also in agreement with the experimental results of Bierig *et al.* [3].

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